CLAIMS

What is claimed is:

1. A method for integrated processing of a high Voltage MOSFET device and a split gate MOSFET device comprising the steps of:

providing a substrate comprising a first active region and a second active region, said first and second active device regions comprising a first polysilicon layer overlying the silicon substrate and a silicon nitride layer overlying the first polysilicon layer;

photolithographically patterning and etching through a thickness portion of the silicon nitride layer to expose a portion of the first polysilicon layer in the second active region;

forming a first portion of a dielectric layer overlying the polysilicon portion while blocking oxide growth over the first active region;

etching selected portions of the silicon nitride layer and first polysilicon layer to form exposed portions of the silicon substrate over the first active region while leaving the second active region unetched; and,

forming a gate dielectric layer over the exposed portions of the substrate in the first active region to a predetermined thickness while simultaneously forming a second portion of the dielectric layer over the second active region to form the dielectric layer at a final predetermined thickness.

2. The method of claim 1, further comprising the steps of:

photolithographically patterning and etching through a thickness of the silicon nitride layer and the polysilicon layer in the first and second active regions to form a first polysilicon electrode in the second active region;

thermally growing a third oxide layer over exposed portions of the first polysilicon electrode;

blanket depositing a second polysilicon layer; and,

photolithographically patterning and etching through a thickness of the second polysilicon layer to form second polysilicon electrodes over the first and second active regions.

3. The method of claim 1, wherein the first active region comprises a high voltage MOSFET for operation at a voltage of from about 30 Volts to about 60 Volts.

4. The method of claim 3, wherein the first active region includes electrically isolating field oxide LOCOS structures.

5. The method of claim 1, wherein the gate oxide layer and the second portion of the oxide layer are formed to a thickness of from about 800 to about 1200 Angstroms.

6. The method of claim 5, wherein the first portion of the oxide layer is formed at a thickness of about 800 to about 1200 Angstroms.

7. The method of claim 1, wherein the polysilicon layer is formed at a thickness of about 1000 Angstroms to about 2000 Angstroms.

8. The method of claim 1, wherein the silicon nitride layer is formed at a thickness of about 1000 Angstroms to about 3000 Angstroms.

9. The method of claim 2, further comprising an ion implantation step over active region B prior to growing the first oxide layer and over active region A prior to thermally growing the gate oxide layer.

10. The method of claim 2, wherein the second polysilicon layer comprises an in-situ doped amorphous layer.

11. The method of claim 1, wherein the first polysilicon electrode comprises a floating gate electrode in a split gate configuration.

12. The method of claim 2, wherein the second polysilicon electrode over the second active region comprises a wordline polysilicon electrode formed adjacent the first polysilicon electrode.

13. A method for integrated processing of a high Voltage MOSFET device and a split gate MOSFET device comprising the steps of:

providing a silicon process wafer comprising a first active region for HV MOSFET device formation including isolation

structures and a second active device region for forming split-gate MOSFET flash memory devices;

blanket depositing a first polysilicon layer;

blanket depositing a silicon nitride layer over and contacting the polysilicon layer;

photolithographically patterning and etching through a thickness portion of the silicon nitride layer to form an exposed polysilicon portion of the polysilicon layer in the second active region;

growing a first oxide layer portion overlying the exposed polysilicon portion to a first predetermined thickness while blocking oxide growth over the first active region;

photolithographically patterning and etching selected portions of the silicon nitride layer and the polysilicon layer over the first active region to form exposed silicon portions of the silicon wafer;

thermally growing a gate oxide over the exposed silicon portions to a predetermined thickness while simultaneously growing a second oxide layer portion over the first oxide layer portion to form an oxide spacer at a final predetermined thickness; and,

etching through a thickness of the silicon nitride layer and the polysilicon layer to form a first polysilicon electrode underlying the oxide spacer.

14. The method of claim 13, further comprising the steps of:

forming source and drain regions in the first active region;

growing a third oxide layer over exposed portions of the first polysilicon electrode;

blanket depositing a second polysilicon layer; and,

photolithographically patterning and etching the second polysilicon layer to form second polysilicon electrodes over the first and second active regions.

15. The method of claim 13, wherein the first active region comprises a silicon substrate region for forming high voltage MOSFETS operating at a voltage of from about 30 Volts to about 60 Volts.

16. The method of claim 13, wherein the gate oxide layer and second oxide layer portions are formed to a thickness of from

about 800 to about 1200 Angstroms.

17. The method of claim 13, wherein the first oxide layer portion is formed at a thickness of about 800 to about 1200 Angstroms.

18. The method of claim 13, further comprising an ion implantation step prior to the steps of growing a first oxide layer portion and thermally growing a gate oxide layer.

19. The method of claim 13, wherein the first polysilicon electrode comprises a floating gate electrode in a split gate configuration.

20. The method of claim 14, wherein the second polysilicon electrode over the second active region comprises a wordline polysilicon electrode formed adjacent the first polysilicon electrode.